

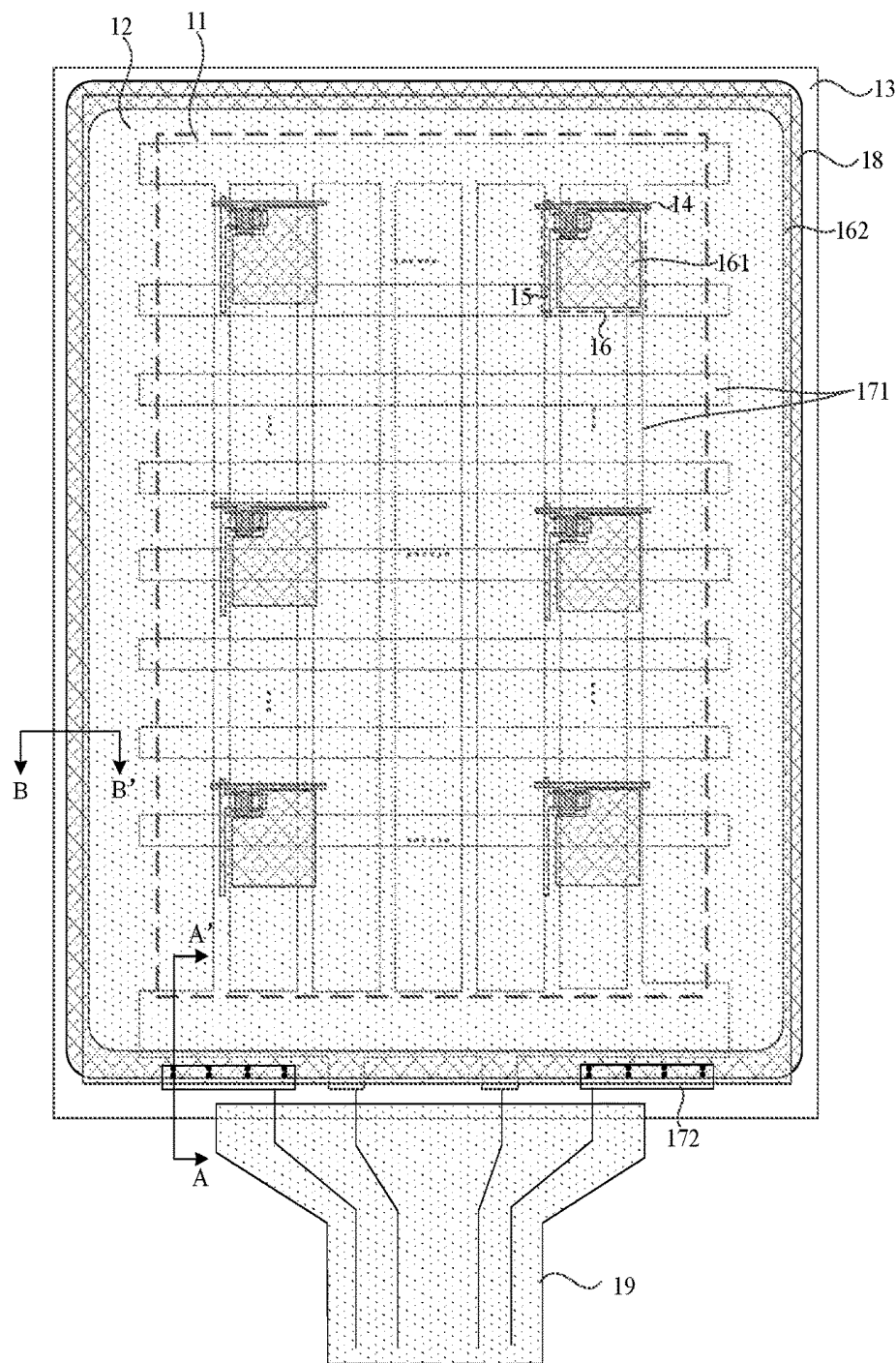


FIG. 1

(Prior Art)

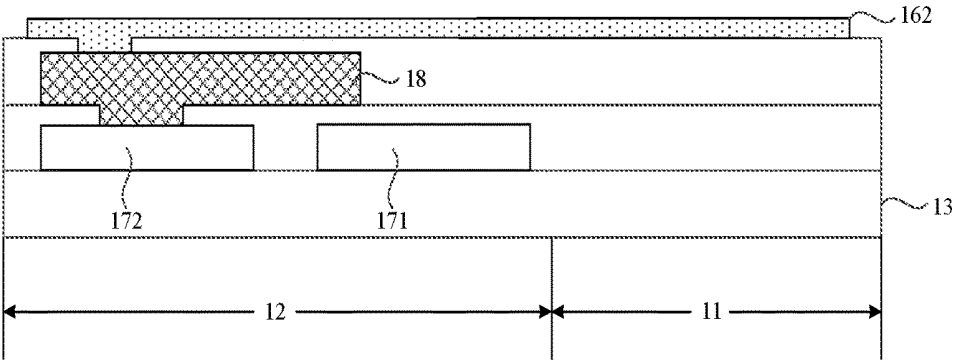


FIG. 2
(Prior Art)

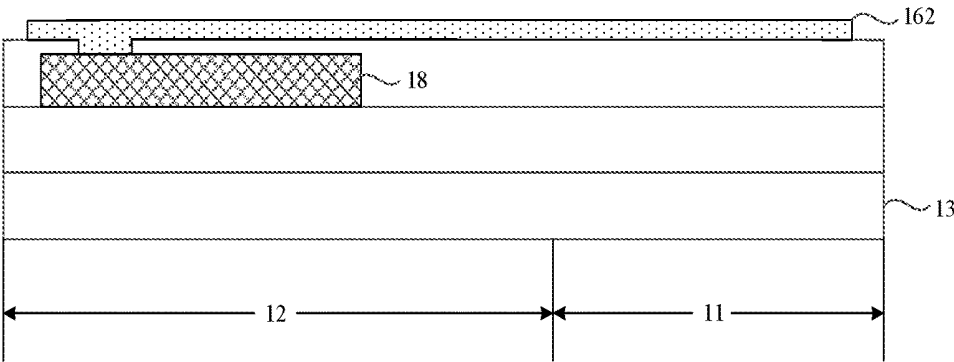


FIG. 3
(Prior Art)

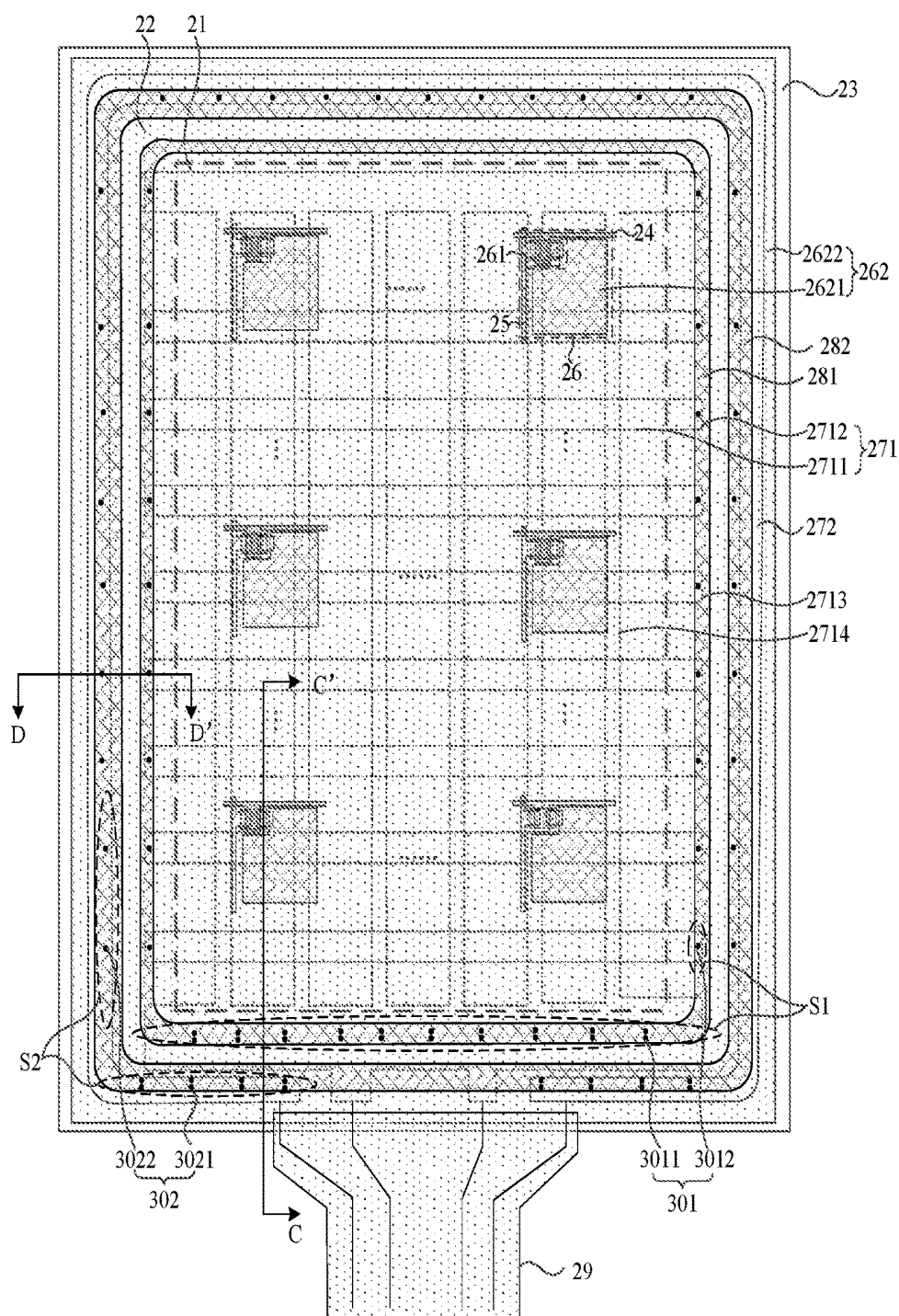


FIG. 4

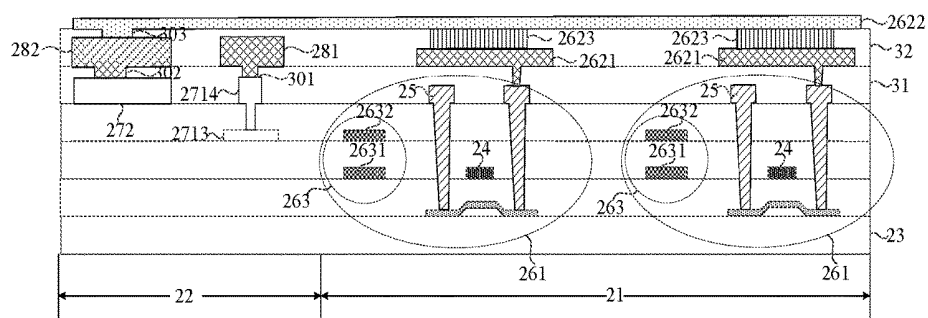


FIG. 5

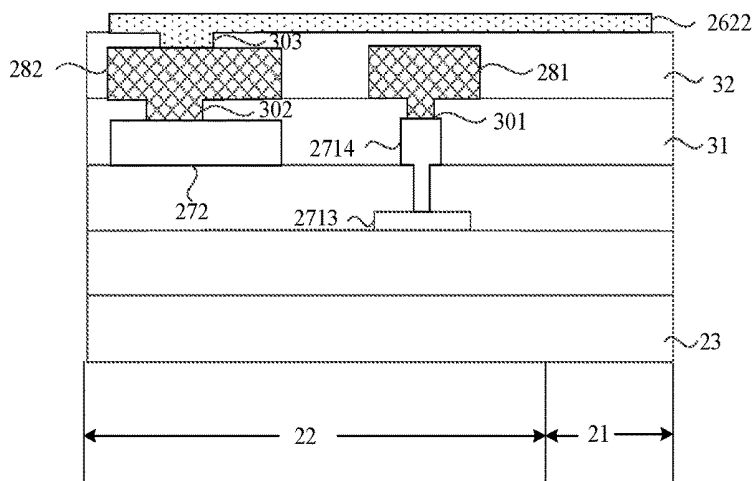


FIG. 6

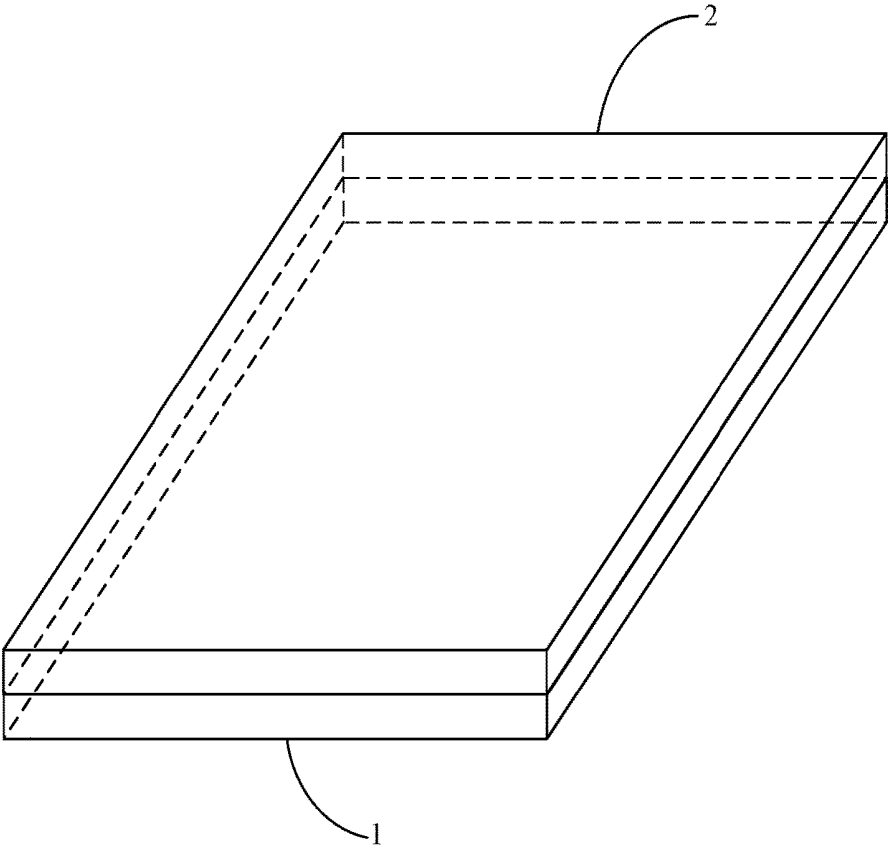


FIG. 7

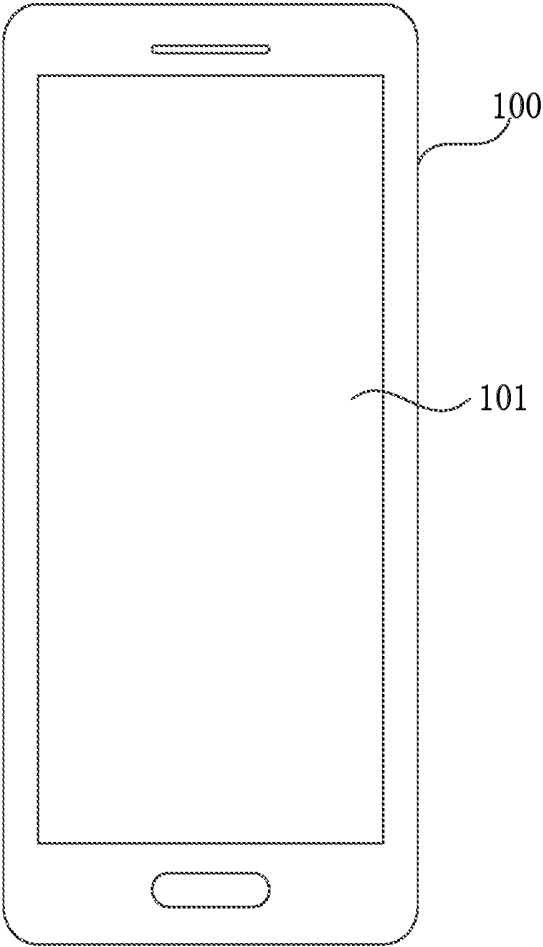


FIG. 8

**ARRAY SUBSTRATE, ORGANIC LIGHT
EMITTING DISPLAY PANEL AND ORGANIC
LIGHT EMITTING DISPLAY DEVICE**

**CROSS-REFERENCES TO RELATED
APPLICATIONS**

[0001] This application claims priority to Chinese patent application No. CN201711172127.1, filed on Nov. 22, 2017, the disclosure of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] Embodiments of the present disclosure relate to the field of semiconductor technologies, and, in particular, relate to an array substrate, an organic light emitting display panel and an organic light emitting display device.

BACKGROUND

[0003] In recent years, Organic Light-Emitting Diodes (OLEDs) have become a very popular emerging flat panel display product in China and abroad, because OLED displays have the advantages such as self-luminous, wide viewing angle, short reaction time, high luminous efficiency, low operating voltage, thin thickness, large size, flexibility, and simple fabrication process. Moreover, OLED displays have the potential of low cost.

[0004] OLEDs can be divided into two categories according to their driving modes: passive driving OLEDs and active driving OLEDs, also known as direct addressing OLEDs and thin film transistor (TFT) matrix addressing OLEDs. Active driving OLEDs are also known as active matrix (AMOLEDs) types. Each light-emitting unit in an AMOLED has a TFT for independent addressing control. A display pixel composed of a light-emitting unit and a TFT addressing circuit needs a power signal wire which applies a direct current signal to drive the pixel.

[0005] However, in a large-size AMOLED display device, since the backplane power signal line has a certain resistance R and the drive currents I of these pixels are provided by the power signal, the power voltage received by a region close to the supply position of the power signal is higher than the power voltage received by a region a distance away from the supply position of the power signal. This phenomenon is referred to as IR drop. IR Drop will cause current differences in different regions, affecting the display effect of the device display.

SUMMARY

[0006] In view of this, embodiments of the present disclosure provide an array substrate, a display panel and a display device so as to a technical issue of poor display effect caused by IR drop on the power signal line in the related art.

[0007] According to a first aspect, embodiments of the present disclosure provide an array substrate. The array substrate includes: a display region and a non-display region surrounding the display region; a base substrate; a plurality of scan lines and a plurality of data lines; a first electrode wire and a second electrode wire; and a first metal wire and a second metal wire.

[0008] The plurality of scan lines and the plurality of data lines are formed on a side of the base substrate. The plurality of scan lines are insulated from the plurality of data lines, the

plurality of scan lines intersect the plurality of data lines to form a plurality of pixel units. Each of the plurality of pixel units includes a driving circuit layer and an organic light-emitting device layer which are successively formed on the base substrate, and the organic light-emitting device layer includes an anode layer and a cathode layer.

[0009] The first electrode wire and the second electrode wire are formed at the side of the base substrate. The first electrode wire is configured to provide a first supply voltage signal for the anode layer, and the second electrode wire is configured to provide a second supply voltage signal for the cathode layer. The first electrode wire includes a first part in the display region and a second part extending into the non-display region. The second electrode wire is formed in the non-display region and surrounds the display region.

[0010] The first metal wire and the second metal wire are formed in the non-display region and surround the display region. The first metal wire and the second metal wire are electrically insulated from each other, the first metal wire is at a side of the second metal wire close to the display region, the first metal wire is electrically connected to the second part of the first electrode wire, and the second metal wire is electrically connected to the second electrode wire.

[0011] According to a second aspect, embodiments of the present disclosure provide a display panel including the array substrate in the first aspect.

[0012] According to a third aspect, embodiments of the present disclosure provide a display device including the display panel in the second aspect.

[0013] According to the array substrate, display panel and display device provided by embodiments of the present disclosure, the first electrode wire and the second electrode wire are formed at a side of the base substrate, the first electrode wire is configured to provide the first supply voltage signal for the anode layer, and the second electrode wire is configured to provide the second supply voltage signal for the cathode layer, the first metal wire and the second metal wire which are electrically insulated from each other are formed in a part of the non-display region surrounding the display region, the first metal wire is at the side of the second metal wire close to the display region, the first metal wire is electrically connected to the first electrode wire, and the second metal wire is electrically connected to the second electrode wire, thereby reducing IR drops of supply voltage signals on the first electrode wire and the second electrode wire and improving the display effect. Moreover, the metal wire which is separately arranged in the related art is divided to the first metal wire and second metal wire, such that the stress on the first metal wiring and the second metal wiring can be also reduced, thereby improving the encapsulation effect of the display panel.

BRIEF DESCRIPTION OF DRAWINGS

[0014] To describe the technical solutions in the exemplary embodiments of the present disclosure more clearly, accompanying drawings for describing the embodiments are briefly described. Apparently, these accompanying drawings are only the accompanying drawings of a part of embodiments to be described rather than all accompanying drawings. Those of ordinary skill in the art can derive other drawings from these accompanying drawings without creative efforts.

[0015] FIG. 1 is a schematic top view of an array substrate in the prior art.

[0016] FIG. 2 is a schematic cross-sectional view of the array substrate shown in FIG. 1 taken along a cross section line A-A'.

[0017] FIG. 3 is a schematic cross-sectional view of the array substrate shown in FIG. 1 taken along a cross section line B-B'.

[0018] FIG. 4 is a schematic top view of an array substrate according to an embodiment of the present disclosure.

[0019] FIG. 5 is a schematic cross-sectional view of the array substrate shown in FIG. 4 taken along a cross section line C-C'.

[0020] FIG. 6 is a schematic cross-sectional view of the array substrate shown in FIG. 4 taken along a cross section line D-D'.

[0021] FIG. 7 is a schematic perspective view of a display panel according to an embodiment of the present disclosure.

[0022] FIG. 8 is a schematic top view of a display device according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0023] To make the objectives, technical solutions, and advantages of the present disclosure clearer, the technical solutions of the present disclosure will be fully described below through specific embodiments with reference to the accompanying drawings in the embodiments. Apparently, the described embodiments are merely some but not all embodiments of the present disclosure. All other embodiments obtained by persons of ordinary skill in the art based on the embodiments of the present disclosure without creative efforts will fall within the protection scope of the present disclosure.

[0024] FIG. 1 is a schematic top view of an array substrate in the prior art. FIG. 2 is a schematic cross-sectional view of the array substrate shown in FIG. 1 taken along a section line A-A'. FIG. 3 is a schematic cross-sectional view of the array substrate shown in FIG. 1 taken along a section line B-B'. As shown in FIG. 1, FIG. 2 and FIG. 3, the array substrate may include a display area 11 and a non-display area 12 surrounding the display area 11.

[0025] The array substrate further includes: a base substrate 13, a plurality of scan lines 14 and a plurality of data lines 15; a first electrode wire 171 and a second electrode wire 172; and a metal wire 18.

[0026] The plurality of scan lines 14 and the plurality of data lines 15 are formed at a side of the base substrate 13. The plurality of scan lines 14 are insulated from the plurality of data lines 15. The plurality of scan lines 14 intersect the plurality of data lines 15 to form a plurality of pixel units 16. Each of the plurality of pixel units 16 includes an anode layer 161 and a cathode layer 162. FIG. 1 illustrates the cathode layer 162 as an entire plane electrode as an example.

[0027] The first electrode wire 171 and the second electrode wire 172 are formed at the side of the base substrate 13. Both of the first electrode wire 171 and the second electrode wire 172 are electrically connected to a flexible printed circuit (FPC) board 19 in the non-display region 12. The first electrode wire 171 receives a first supply voltage signal provided by the FPC 19, and the second electrode wire 172 receives a second supply voltage signal provided by the FPC 19. The first electrode wire 171 is configured to provide the first supply voltage signal for the anode layer 161, and the second electrode wire 172 is configured to provide the second supply voltage signal for the cathode layer 162.

[0028] The metal wire 18 is formed in the non-display region 12 and surrounds the display region 11. The metal wire 18 is electrically connected to the cathode layer 162 through a via. The metal wire 18 is electrically connected to the second electrode wire 172 at a lower edge of the array substrate through another via, and is configured to transmit the second supply voltage signal on the second electrode wire 172 to the cathode layer 162.

[0029] As shown in FIG. 1, in the related art, in order to reduce the influence of the IR drop caused by the first electrode wire 171, the first electrode wire 171 generally has a uniform mesh design for increasing the connection relationship between the pixels and evenly sharing resistances and currents. In this way, each pixel unit 16 receives a same or similar first voltage signal. With continued reference to FIG. 1, the second electrode wire 172 is only at the side of the non-display area 12 close to the FPC 19. The second electrode wire 172 is electrically connected to the metal wire 18 at the lower edge of the array substrate, and supply the second supply voltage signal to the cathode layer 162 through the metal wire 18.

[0030] It should be noted that, both the first supply voltage signal and the second supply voltage signal are provided by the FPC 19 in the non-display region 12, so even the first electrode wire 171 is designed to have the mesh structure, there is still a big difference between the first supply voltage signals received by pixel units 16 in the display region 11 where the pixel units 16 have different distances from the FPC 19, causing IR drop and affecting the display uniformity of the display panel. Likewise, the metal wire 18 is electrically connected to the second electrode wire 172 only through the via at the lower edge of the array substrate, so the second supply voltage signal on the metal wire 18 also has a large IR drop, and the loss of the second supply voltage signal on the metal wire 18 is large, affecting the display effect of the display panel.

[0031] Based on the above technical problem, embodiments of the present disclosure provide an array substrate including a display region and a non-display region surrounding the display region. The array substrate further includes: a base substrate; a plurality of scan lines and a plurality of data lines; a first electrode wire and a second electrode wire; and a first metal wire and a second metal wire. The plurality of scan lines and the plurality of data lines are formed at a side of the base substrate. The plurality of scan lines are insulated from the plurality of data lines, the plurality of scan lines intersect the plurality of data lines to form a plurality of pixel units. Each of the plurality of pixel units includes a driving circuit layer and an organic light-emitting device layer which are successively formed on the base substrate, and the organic light-emitting device layer includes an anode layer and a cathode layer. The first electrode wire and the second electrode wire are formed at the side of the base substrate. The first electrode wire is configured to provide a first supply voltage signal for the anode layer, and the second electrode wire is configured to provide a second supply voltage signal for the cathode layer. The first electrode wire includes a first part in the display region and a second part extending into the non-display region. The second electrode wire is formed in the non-display region and surrounds the display region. The first metal wire and the second metal wire are formed in the non-display region and surround the display region. The first metal wire and the second metal wire are electrically insu-

lated from each other, the first metal wire is at a side of the second metal wire close to the display region, the first metal wire is electrically connected to the second part of the first electrode wire, and the second metal wire is electrically connected to the second electrode wire. By the electrical connection of the first metal wire and the second part of the first electrode wire and the electrical connection of the second metal wire and the second electrode wire, the resistance of the transmission wire of the first supply voltage signal and the resistance of the transmission wire of the second supply voltage signal are both reduced, thereby reducing the IR drop of the first supply voltage signal on its transmission wire and the IR drop of the second supply voltage signal on its transmission wire and improving the display effect of the display panel. Moreover, the metal wire which is separately arranged in the related arts is divided to the first metal wire and second metal wire, such that the stress on the first metal wiring and the second metal wiring can be also reduced, thereby improving the encapsulation effect of the display panel.

[0032] The technical solutions in embodiments of the present disclosure will be described clearly and completely below with reference to the accompanying drawings in the embodiments. All other embodiments obtained by persons of ordinary skill in the art based on the embodiments of the present disclosure without creative efforts will fall within the protection scope of the present disclosure.

[0033] FIG. 4 is a schematic top view of an array substrate according to an embodiment of the present disclosure. FIG. 5 is a schematic cross-sectional view of the array substrate shown in FIG. 4 taken along a cross section line C-C'. FIG. 6 is a schematic cross-sectional view of the array substrate shown in FIG. 4 taken along a cross section line D-D'. With reference to FIG. 4, FIG. 5 and FIG. 6, the array substrate provided by embodiments of the present disclosure may include a display region 21 and a non-display region 22 surrounding the display region 21.

[0034] The array substrate further includes: a base substrate 23; a plurality of scan lines 24 and a plurality of data lines 25; a first electrode wire 271 and a second electrode wire 272; and a first metal wire 281 and a second metal wire 282.

[0035] The plurality of scan lines 24 and the plurality of data lines 25 are formed at a side of the base substrate 23. The plurality of scan lines 24 are insulated from the plurality of data lines 25, and the plurality of scan lines 24 intersect the plurality of data lines 25 to form a plurality of pixel units 26. Each of the plurality of pixel units 26 includes a driving circuit layer 261 and an organic light-emitting device layer 262 which are successively formed on the base substrate 23. The organic light-emitting device layer 262 includes an anode layer 2621, a cathode layer 2622 and an organic light-emitting layer 2623.

[0036] The first electrode wire 271 and the second electrode wire 272 are formed at the side of the base substrate 23. The first electrode wire 271 is configured to provide a first supply voltage signal for the anode layer 2621. The second electrode wire 272 is configured to provide a second supply voltage signal for the cathode layer 2622. The first electrode wire 271 includes a first part 2711 in the display region 21 and a second part 2712 extending into the non-display region 22. The second electrode wire 272 is formed in the non-display region 22 and surrounds the display region 21.

[0037] The first metal wire 281 and the second metal wire 282 are formed in the non-display region 22 and surround the display region 21. The first metal wire 281 and the second metal wire 282 are electrically insulated from each other. The first metal wire 281 is at a side of the second metal wire 282 close to the display region 21. The first metal wire 281 is electrically connected to the second part 2712 of the first electrode wire 271, and the second metal wire 282 is electrically connected to the second electrode wire 272.

[0038] Optionally, the array substrate may further include an FPC 29 (not shown) in the non-display region 22. The first electrode wire 271 and the second electrode wire 272 are electrically connected to the FPC 29. The first electrode wire 271 is configured to receive the first supply voltage signal provided by the FPC 29, and the second electrode wire 272 is configured to receive the second supply voltage signal provided by the FPC 29. Optionally, the first supply voltage signal is an anode voltage signal PVDD, and the second supply voltage signal is a cathode voltage signal PVEE.

[0039] With continued reference to FIG. 4, the first electrode wire 271 includes a first part 2711 in the display region 21 and a second part 2712 extending into the non-display region 22. The first metal wire 281 which is formed in the non-display region 22 and surrounds the display region 21 is electrically connected to the second part 2712 of the first electrode wire 271. By the electrical connection of the first metal wire 281 and the first electrode wire 271, the area of the transmission wire for conveying the first supply voltage signal is increased, thereby reducing the resistance of the transmission wire for conveying the first supply voltage signal and reducing the IR drop of the first supply voltage signal on the transmission wire. In addition, the first metal wire 281 is arranged in the non-display region 22, and do not occupy the display region 21, thereby not affecting the aperture ratio of the display panel.

[0040] With continued reference to FIG. 4, the second electrode wire 272 is formed in the non-display region 22 and surrounds the display region 21, the second metal wire 282 is also formed in the non-display region 22 and surrounds the display region 21, and the second metal wire 282 is electrically connected to the second electrode wire 272, so the area of the transmission wire for conveying the second supply voltage signal is increased, thereby reducing the resistance of the transmission wire for conveying the second supply voltage signal and reducing the IR drop of the second supply voltage signal on the transmission wire. In addition, both of the second electrode wire 272 and the second metal wire 282 are arranged in the non-display region 22, and do not occupy the display region 21, thereby not affecting the aperture ratio of the display panel.

[0041] It should be noted that, compared with the related art in which only one metal wire disposed in the non-display area 22 is used for transmitting the supply voltage signal, in the embodiment of the present disclosure, the first metal wire 281 and the second metal wire 282 are disposed, and the first metal wire 281 and the second metal wire 282 are insulated from each other, not only reducing the IR drop of the PVDD signal on its signal transmission wire and the IR drop of the PVEE signal on its signal transmission wire, but also reducing the stress bear by the first metal wire 281 and the second metal wire 282 through the insulately arranged first metal wire 281 and the second metal wire 282, thereby ensuring that the first metal wire 281 and the second metal

wire **2821** will not break and improving the overall encapsulation effect of the array substrate.

[0042] Optionally, with continued reference to FIG. 5, the first metal wire **281** and the second metal wire **282** are arranged at a same layer, and the first metal wire **281** and the second metal wire **282** may be arranged at a same layer as the anode layer **2621**. During the fabrication, the first metal wire **281** and the second metal wire **282** may be fabricated by a same process with the anode layer **2621** without any additional fabrication process or mask, ensuring the fabrication process of the first metal wire **281** and the second metal wire **282** simple.

[0043] Optionally, in order to solve the problem of IR drop caused by the first electrode wire **271**, the first electrode wire **271** adopts a uniform mesh design to increase the connection relationship between pixels, and the resistance and the current are equally allocated. With continued reference to FIG. 4, the first electrode wire **271** includes a plurality of first sub-electrode-wires **2713** arranged in an extending direction of the plurality of scan lines **24** and a plurality of second sub-electrode-wires **2714** arranged in an extending direction of the plurality of data lines **25**. The plurality of first sub-electrode-wires **2713** intersect the plurality of second sub-electrode-wires **2714**, and are electrically connected to the plurality of second sub-electrode-wires **2714**. Optionally, the first metal wire **281** may be electrically connected to the plurality of first sub-electrode-wires **2713**; and/or the first metal wire **282** may be electrically connected to the plurality of second sub-electrode-wires **2714**. FIG. 4 merely illustrates an example in which the first metal wire **281** is electrically connected to the first sub-electrode wires **2713** and the second sub-electrode wires **2714**, respectively. As shown in FIG. 4, the first metal wire **281** is electrically connected to the first sub-electrode-wires **2713** near two side edges of the array substrate; and the first metal wire **281** is electrically connected to the second sub-electrode-wires **2714** near the lower edge of the array substrate.

[0044] With continued reference to FIG. 4, in a direction perpendicular to the base substrate **21**, a first region **S1** between the first metal wire **281** and the second part **2712** of the first electrode wire **271** is provided (the first metal wire **281** overlaps the second part **2712** of the first electrode wire **271** in the first region **S1**), and a plurality of first vias **301** are formed in the first region **S1**. The first metal wire **281** is electrically connected to the first electrode wire **271** through the plurality of first vias **301**. In the direction perpendicular to the base substrate **21**, a second region **S2** between the second metal wire and the second electrode wire is provided (the second metal wire overlaps the second electrode wire), and a plurality of second vias **302** are formed in the second region **S2**. The second metal wire **282** is electrically connected to the second electrode wire **272** through the plurality of second vias **302**.

[0045] Exemplarily, the first metal wire **281** is electrically connected to the first electrode wire **271** through the plurality of first vias **301**, ensuring a large contact area between the first metal wire **281** and the first electrode wire **271**, which not only reduces the resistance of the transmission wire conveying the first supply voltage signal, but also ensures that positions with different distances from the FPC **29** have the same or similar voltage drop of the first supply voltage signal, thereby reducing the IR drop of the first supply voltage signal and improving the display uniformity. Likewise, the second metal wire **282** is electrically con-

nected to the second electrode wire **272** through the plurality of second vias **302**, ensuring a large contact area between the second metal wire **282** and the second electrode wire **272**, which not only reduces the resistance of the transmission wire conveying the second supply voltage signal, but also ensures that different positions with respect to the FPC **29** have the same or similar voltage drop of the second supply voltage signal, thereby reducing the IR drop of the second supply voltage signal and improving the display uniformity.

[0046] Specifically, with continued reference to FIG. 4, the plurality of first vias **301** may include a plurality of first type vias **3011** arranged in the extending direction of the plurality of scan lines **24** and a plurality of second type vias **3012** arranged in the extending direction of the plurality of data lines **25**, the first metal wire **281** is electrically connected to the plurality of first sub-electrode wires **2713** through the plurality of second type vias **3012**, and the first metal wire **281** is electrically connected to the plurality of second sub-electrode wires **2714** through the plurality of first type vias **3011**. Further, the plurality of second vias **302** may include a plurality of third type vias **3021** arranged in the extending direction of the plurality of scan lines **24** and a plurality of fourth type vias **3022** arranged in the extending direction of the plurality of data lines **25**, and the second metal wire **282** is electrically connected to the second electrode wire **272** through the plurality of third type vias **3021** and the plurality of fourth type vias **3022**.

[0047] Optionally, since the plurality of first sub-electrode wires **2713** are arranged in the extending direction of the scan lines **24**, each of the plurality of first sub-electrode wires **2713** may be arranged to correspond to a respective one of the plurality of scan lines **24**. In this way, the arrangement of the plurality of first sub-electrode wires **2713** will not affect the aperture ratio of the display panel. Each of the plurality of first sub-electrode wires **2713** corresponds to a respective one of the plurality of scan lines **24**, each of the plurality of scan lines **24** corresponds to a row of pixel units **26**, and the first metal wire **281** is electrically connected to the plurality of first sub-electrode wires **2713** through the plurality of second type vias **3012**, so in the actual design process, each of the second type of vias **3012** may correspond to a respective row of pixel units **26**.

[0048] Optionally, with continued reference to FIG. 5, the driving circuit layer **261** provided by embodiments of the present disclosure may further include a storage capacitor **263**. The storage capacitor **263** includes a first plate **2631** and a second plate **2632**. In one or more embodiments, the first sub-electrode-wires **2713** may be arranged at a same layer as the scan lines **24**. In one or more embodiments, alternatively, the first sub-electrode wires **2713** may be arranged at a same layer as the first plate **2631** or the second plate **2632**. In one or more embodiments, the second sub-electrode-wires **2714** may be arranged at a same layer as the data lines **25**. FIG. 5 merely exemplarily illustrates a configuration in which the first sub-electrode-wires **2713** is arranged at a same layer as the second plate **2632** as an example. By configuring the first sub-electrode-wires **2713** at the same layer as the scan lines **24**, or the first plate **2631**, or the second plate **2632** and configuring the second sub-electrode-wires **2714** at the same layer as the data lines **25**, it is ensured that, the first sub-electrode-wires **2713** are fabricated in the same fabrication process step with the scan lines **24**, or the first plate **2631**, or the second plate **2632** during fabrication, and the second sub-electrode-wires **2714**

are fabricated in the same fabrication process step with the data lines **25** during fabrication, which is compatible with the existing array substrate fabrication process and ensures a simple fabrication process. It should be noted that, since the scan line **24** and a gate electrode in the driving circuit layer **261** are arranged at the same layer and connected to each other, the scan line **24** is represented by the gate electrode in FIG. 5. Similarly, since the data line **25** and a source electrode in the driving circuit layer **261** are arranged at the same layer and connected to each other, the data line **25** is represented by the source electrode in FIG. 5.

[0049] Optionally, the second electrode wire **272** may be arranged at a same layer as the data lines **25** (not shown), the second electrode wire **272** and the data lines **25** may be fabricated in a same fabrication process step during fabrication, which is compatible with the existing array substrate fabrication process and ensures a simple fabrication process.

[0050] Optionally, with continued reference to FIG. 5, the array substrate provided by embodiments of the present disclosure may further include a planarization layer **31** between the driving circuit layer **261** and the organic light-emitting layer **262**. The planarization layer **31** may protect the driving circuit layer **261** underneath the planarization layer **31**. Optionally, the planarization layer **31** may be made from organic material including Benzocyclobutene or Acrylic acid or inorganic material including silicon nitride. The planarization layer **31** may be formed as a single layer, a double layer, or multiple layers. Optionally, since the first metal wire **281** and the second metal wire **282** may be arranged at a same layer as the anode layer **2621**, the first vias **301** by which the first metal wire **281** and the first electrode wire **272** are connected may be formed in the planarization layer **31**. Similarly, the second vias **302** by which the second metal wire **282** and the second electrode wire **272** are connected may also be formed in the planarization layer **31**. The configuration in which the first vias **301** and the second vias **302** are formed in the planarization layer **31** ensures that the fabrication of the first vias **301** and the second vias **302** is simple and is compatible with the existing array substrate fabrication process.

[0051] Optionally, with continued reference to FIG. 5, the array substrate provided by embodiments of the present disclosure may further include a pixel definition layer **32** between the anode layer **2621** and the cathode layer **2622**. The pixel definition layer **32** is located between two adjacent pixel units **16**, and can prevent or reduce mixing of colors of adjacent pixel units. Optionally, the material of the pixel definition layer **32** may include one or more organic insulation materials such as Polyimides, Polyamide resin, Acrylic resin, Benzocyclobutene and phenolic resin. The material of the pixel definition layer **32** may further include one or more inorganic insulation materials such as SiO₂, SiNx, Al₂O₃, CuOx, Tb₄O₇, Y₂O₃, Nb₂O₅ and Pr₂O₃. In addition, the pixel definition layer **32** may also have a multi-layer structure in which organic insulation materials and inorganic insulation materials are alternately arranged. A cathode contacting hole **303** is formed at the pixel definition layer **32**. The cathode layer **2622** and the second metal wire **282** are electrically connected to each other through the cathode contacting hole **303**. By forming the cathode contacting hole **303** at the pixel definition layer **32** and electrically connecting the cathode layer **2622** and the second metal wire **282** through the cathode contacting hole **303**, it is ensured that the formation of the cathode contact-

ing hole **303** is simple and is compatible with the existing array substrate fabrication process.

[0052] FIG. 7 is a schematic structural view of a display panel according to an embodiment of the present disclosure. As shown in FIG. 7, the display panel provided by embodiments of the present disclosure includes the array substrate **1** in the above embodiments and a counter substrate **2** opposite to the array substrate **1**. The counter substrate **2** may be a cover plate or other encapsulation layer.

[0053] FIG. 8 is a schematic structural view of a display device according to an embodiment of the present disclosure. As shown in FIG. 8, the display device **100** may include the display panel **101** in any embodiment of the present disclosure. The display device **100** may be a phone shown in FIG. 8, or may be a computer, a television, a smart wearable display device, and the like, which is not specifically limited in embodiments of the present disclosure.

[0054] It should be noted that the above is only the optional embodiments of the present disclosure and the applied technical principles. Those skilled in the art should understand that the present disclosure is not limited to the specific embodiments described herein, and various apparent modification, readjustments, combinations and substitutions can be made by those skilled in the art without departing from the scope of the present disclosure. Therefore, although the present disclosure has been described in detail by way of the above embodiments, the present disclosure is not limited only to the above embodiments, and may include more other equivalent embodiments without departing from the concept of the present disclosure. However, the scope of the present disclosure is determined by the scope of the appended claims.

What is claimed is:

1. An array substrate, comprising:

- a display region and a non-display region surrounding the display region;
- a base substrate;
- a plurality of scan lines and a plurality of data lines, formed on a side of the base substrate, wherein the plurality of scan lines are insulated from the plurality of data lines, the plurality of scan lines intersect the plurality of data lines to form a plurality of pixel units, wherein each of the plurality of pixel units comprises a driving circuit layer and an organic light-emitting device layer which are successively formed on the base substrate, and wherein the organic light-emitting device layer comprises an anode layer and a cathode layer;
- a first electrode wire and a second electrode wire, formed at the side of the base substrate, wherein the first electrode wire is configured to provide a first supply voltage signal for the anode layer, the second electrode wire is configured to provide a second supply voltage signal for the cathode layer, wherein the second electrode wire is formed in the non-display region and surrounds the display region; and
- a first metal wire and a second metal wire, formed in the non-display region and surround the display region, wherein the first metal wire and the second metal wire are electrically insulated from each other, wherein the first metal wire is at a side of the second metal wire close to the display region, wherein the first metal wire is electrically connected to the first electrode wire, and wherein the second metal wire is electrically connected to the second electrode wire.

2. The array substrate according to claim 1, wherein the first metal wire and the second metal wire are arranged in a same layer as the anode layer.

3. The array substrate according to claim 1, wherein the first electrode wire comprises a plurality of first sub-electrode-wires arranged in an extending direction of the plurality of scan lines, and a plurality of second sub-electrode-wires arranged in an extending direction of the plurality of data lines;

wherein each sub-electrode-wire of the plurality of first sub-electrode-wires and the plurality of second sub-electrode-wires comprises a first part in the display region and a second part extending into the non-display region; and

wherein the first metal wire is electrically connected to the second parts of the plurality of the first sub-electrode wires; and

wherein the plurality of first sub-electrode-wires intersect the plurality of second sub-electrode-wires.

4. The array substrate according to claim 3, wherein the first metal wire is electrically connected to the plurality of first sub-electrode-wires.

5. The array substrate according to claim 3, wherein the first metal wire is electrically connected to the plurality of second sub-electrode-wires.

6. The array substrate according to claim 3, wherein the first metal wire is electrically connected to the plurality of first sub-electrode-wires and the plurality of second sub-electrode-wires.

7. The array substrate according to claim 4, wherein, the first metal wire overlays the second parts of the plurality of first sub-electrode wires in a first region, and the second metal wire overlays the second electrode wire in a second region.

8. The array substrate according to claim 7, wherein the first metal wire is electrically connected to the first electrode wire through a plurality of first vias in the first region, and the second metal wire is electrically connected to the second electrode wire through a plurality of second vias in the second region.

9. The array substrate according to claim 8, wherein the plurality of first vias comprise a plurality of first type vias arranged in the extending direction of the plurality of scan lines, and a plurality of second type vias arranged in the extending direction of the plurality of data lines, wherein the first metal wire is electrically connected to the plurality of first sub-electrode wires through the plurality of second type vias, and the first metal wire is electrically connected to the plurality of second sub-electrode-wires through the plurality of first type vias;

wherein the plurality of second vias comprise a plurality of third type vias arranged in the extending direction of the plurality of scan lines and a plurality of fourth type vias arranged in the extending direction of the plurality of data lines; and

wherein the second metal wire is electrically connected to the second electrode wire through the plurality of third type vias and the plurality of fourth type vias.

10. The array substrate according to claim 9, wherein each of the plurality of second type vias is arranged to correspond to a respective row of pixel units.

11. The array substrate according to claim 3, wherein the driving circuit layer further comprises a storage capacitor having a first plate and a second plate,

wherein the plurality of first sub-electrode-wires are arranged in a same layer as the plurality of scan lines; wherein the plurality of second sub-electrode-wires are arranged in a same layer as the plurality of data lines.

12. The array substrate according to claim 3, wherein the driving circuit layer further comprises a storage capacitor having a first plate and a second plate,

wherein the plurality of first sub-electrode-wires are arranged in a same layer as the first plate of the storage capacitor;

wherein the plurality of second sub-electrode-wires are arranged in a same layer as the plurality of data lines.

13. The array substrate according to claim 1, wherein the second electrode wire is arranged in a same layer as the plurality of data lines.

14. The array substrate according to claim 8, further comprising a planarization layer between the driving circuit layer and the organic light-emitting layer, wherein the plurality of first vias and the plurality of second vias are formed in the planarization layer.

15. The array substrate according to claim 1, further comprising a pixel definition layer between the anode layer and the cathode layer, wherein the pixel definition layer is provided with a cathode contacting hole, and wherein the cathode layer is electrically connected to the second metal wire through the cathode contacting hole.

16. A display panel, comprising: an array substrate, wherein the array substrate comprises:

a display region and a non-display region surrounding the display region;

a base substrate;

a plurality of scan lines and a plurality of data lines, formed on a side of the base substrate, wherein the plurality of scan lines are insulated from the plurality of data lines, the plurality of scan lines intersect the plurality of data lines to form a plurality of pixel units, wherein each of the plurality of pixel units comprises a driving circuit layer and an organic light-emitting device layer which are successively formed on the base substrate, and wherein the organic light-emitting device layer comprises an anode layer and a cathode layer;

a first electrode wire and a second electrode wire, formed at the side of the base substrate, wherein the first electrode wire is configured to provide a first supply voltage signal for the anode layer, the second electrode wire is configured to provide a second supply voltage signal for the cathode layer, wherein the second electrode wire is formed in the non-display region and surrounds the display region; and

a first metal wire and a second metal wire, formed in the non-display region and surround the display region, wherein the first metal wire and the second metal wire are electrically insulated from each other, wherein the first metal wire is at a side of the second metal wire close to the display region, wherein the first metal wire is electrically connected to the first electrode wire, and wherein the second metal wire is electrically connected to the second electrode wire.

17. A display device, comprising: a display panel, wherein the display panel comprises an array substrate, and wherein the array substrate comprises:

a display region and a non-display region surrounding the display region;

a base substrate;

- a plurality of scan lines and a plurality of data lines, formed on a side of the base substrate, wherein the plurality of scan lines are insulated from the plurality of data lines, the plurality of scan lines intersect the plurality of data lines to form a plurality of pixel units, wherein each of the plurality of pixel units comprises a driving circuit layer and an organic light-emitting device layer which are successively formed on the base substrate, and wherein the organic light-emitting device layer comprises an anode layer and a cathode layer;
- a first electrode wire and a second electrode wire, formed at the side of the base substrate, wherein the first electrode wire is configured to provide a first supply voltage signal for the anode layer, the second electrode wire is configured to provide a second supply voltage signal for the cathode layer, wherein the second electrode wire is formed in the non-display region and surrounds the display region; and
- a first metal wire and a second metal wire, formed in the non-display region and surround the display region, wherein the first metal wire and the second metal wire are electrically insulated from each other, wherein the first metal wire is at a side of the second metal wire close to the display region, wherein the first metal wire is electrically connected to the first electrode wire, and wherein the second metal wire is electrically connected to the second electrode wire.

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专利名称(译)	阵列基板，有机发光显示面板和有机发光显示装置		
公开(公告)号	US20180226460A1	公开(公告)日	2018-08-09
申请号	US15/944465	申请日	2018-04-03
[标]申请(专利权)人(译)	上海天马AM OLED		
申请(专利权)人(译)	上海天马AM-OLED CO. , LTD.		
当前申请(专利权)人(译)	上海天马AM-OLED CO. , LTD.		
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摘要(译)

提供一种阵列基板，有机发光显示面板和有机发光显示装置。阵列基板包括基础基板和像素单元;第一电极线和第二电极线形成在基础基板的一侧，第一电极线被配置为为阳极层提供第一电源电压信号，第二电极线被配置为提供第二电源电压信号阴极层;第一金属线和第二金属线形成在非显示区域中并围绕显示区域。第一金属线电连接到第一电极线，第二金属线电连接到第二电极线。

